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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/389,393	09/03/1999	HISASHI OHTANI	07977/204002	5375

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EXAMINER
BAUMEISTER, BRADLEY W

ART UNIT	PAPER NUMBER
2815	20

DATE MAILED: 06/14/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/389,393	Ohtani et al.
Examiner	**Art Unit**
B. William Baumeister	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *May 9, 2002*.

2a) ☐ This action is **FINAL.** 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-3, 6-8, 11-13, 15-18, 20-23, 25-27, and 29-38* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1-3, 6-8, 11-13, 15-18, 20-23, 25-27, and 29-38* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☒ The proposed drawing correction filed on *Feb 28, 2002* is: a) ☐ approved b) ☒ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Allowable Subject Matter

1. The indicated allowability of the claims is withdrawn in view of the newly discovered reference(s) to Ota, JP '615. Rejections based on the newly cited reference(s) follow.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the bottom-gate (gate formed below the channel) embodiment set forth in claims 21, 25 and their dependent claims must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Claim Objections

3. Claim 31 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Independent claim 25 has been amended to recite that the second insulating film comprises oxide of said first and second conductive layers. As such, dependent claim 31--reciting that said [sic: second] insulating film comprises anodization oxide of said first and second conductive layers--does not appear to further limit the claim.

a. Applicant is required to either (1) provide an explanation of why "anodization oxide" of claim 31 further limits the recited oxide structure of claim 25, in light of the examiner's

understanding that "anodization" merely recites the method by which the oxide was formed; or alternatively (2) cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 21-23, 25-27, 31, 32, 37 and 38 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

a. Each one of independent claims 21 and 25 is directed towards a bottom gate-type TFT transistor (i.e., channel-over-gate-on-insulating substrate) and sets forth "a first insulating film formed on said gate electrode," and "a second insulating film comprising oxide of said first and second conductive layers..." As such, the anodic oxide insulating films of both of the two-layer gate structure are set forth as together composing the second insulating film. Each of dependent claims 22 and 26 further defines the first insulating film as being composed of SiOx. The question remains (see Office Action #15, dated 12/22/2001) of where the specification

provides support for the recitation of an additional first insulating film formed on the gate electrode.

b. Applicant has asserted (REMARKS, page 4; paper #17, entered 5/22/2002) that support is found at page 11, lines 14-17. This is not accurate. This portion of the specification is directed towards a top gate-type TFT, and the SiOx gate insulating film referenced at page 11 is one that is interposed between the gate and the underlying channel. In that embodiment, the gate is oxidized and the resultant anodic insulation layers are formed on the sides and the top of the gate--opposite to the side of the gate having the SiOx insulating layer.

However, in a bottom gate-type TFT, the gate is formed on an insulating substrate, and the top and sides are oxidized. Then a channel (poly) layer is formed over the anodic oxide insulation. Thus, there is no need for an additional SiOx insulating layer to also be formed between the gate and the channel, since the anodic oxide is already there. More importantly, the only mention of a bottom gate-type structure is set forth at page 14 of the specification, which solely states:

> For example, while a top-gate type thin film transistor has been disclosed in the preferred embodiment, the present invention can be applied to a bottom gate type transistor in which a gate electrode is located below the channel forming region.

This disclosure contains no mention of employing a SiOx gate oxide in addition to the anodic oxides in between the channel and gate in a bottom-gate TFT. As such, the inclusion of the limitations relating to the first insulating layer constitutes new matter.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 26, 31 and 32 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. Independent claim 25 sets forth "a first insulating film formed on said gate electrode" (line 5) and subsequently "a second insulating film comprising oxide of said first and second conductive layers" (lines 9-10). Each of dependent claims 26, 31 and 32 recite "...wherein said insulating film is a gate insulating film comprising silicon oxide." There is insufficient antecedent basis for "said insulating film" in claim these dependent claims, rendering them indefinite.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 21, 23, 27, 31 and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Ota, JP '615 (English abstract, JPO machine-translation, and USPTO translation of [0018]

enclosed herewith). Ota discloses a bottom-gate TFT comprising the following layers formed on an insulating substrate: Al gate layer 12 having the side portions 18 anodized to form AlOx; a Ta layer 14, most of which has been oxidized to form TaOx layer 20 (please note the Abstract and paragraph [0018] which recite that most--not all--of the Ta is oxidized); SiN insulating film 22; and Si film 24.

a. Regarding claims 23 and 27, while it is unclear from the JPO machine translation whether Ota expressly recites that the carrier or conductive layer 24 is composed of Si, one skilled in the art would understand that this is implied because Si is what is employed for such TFT S/channel/D layers. Further, while it is also unclear from the translation whether the reference expressly recites that the conductive layer is polycrystalline, this fact is inherently implies since the Si layer is formed on the insulating layer and as such could not be monocrystalline.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 22 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ota JP '615 as applied to claims 21 and 25 above. Ota discloses that the insulating layer is composed of silicon nitride instead of silicon oxide. It would have been obvious to one of ordinary skill in the art at the time of the invention to have employed SiOx for the insulating layer instead of SiN because SiOx is easier to etch.

12. Claims 1-3, 6-8, 11-13, 15-18, 20, 29, 30 and 33-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ha '530 in view of Ota JP '615 as applied to the claims above.

a. Ha discloses a top-gate poly-Si TFT with a T-shaped, two-layer gate electrode employed for the purpose of reducing drain leakage current. The two-layer gate is composed of a lower oxidizable metal having sufficiently good conductivity characteristics, such as Al or Ta, and the upper gate metal is composed of a material such as chrome [sic: chromium] having an oxidation rate which is lower than that of the first metal, or more specifically, a second material that is not oxidizable. This structure is then covered by an SiOx insulating layer 37. The two gate metal layers are initially deposited so as to have the same dimensional width and is subjected to an anodic oxidation process which causes the lower layer to form an anodic oxide (e.g., AlOx) on the sides of only the lower gate portion, thereby producing a T-shaped gate having a thinner lower metal region that is laterally surrounded by the insulating metal oxide. While Ha teaches that the upper metal layer has a lower oxidation rate for the purpose of producing a T-shaped gate, it does not disclose that the upper metal layer may also be composed of a material wherein

this lower oxidation rate is greater than zero. Further, Ha teaches that the use of chromium presents the problem of erosion during oxidation, and therefore Ha states that it is preferable to further include an additional, patterned protective insulating layer over the chromium layer to protect it during the oxidation process.

b. Ota teaches two-level metal gates that are both oxidizable, and which are, in fact, oxidized, thereby forming an inverted T-shaped gate for a bottom-type TFT. Further, Ota teaches that the upper Ta layer is first etched to have a dimensional width that is less than that of the of lower Al layer, but that upon oxidation some of the Ta--even though originally smaller in the lateral direction--still remains. Thus, this implicitly teaches that Ta has a lower oxidation rate than that of Al. Ota also teaches that while chromium can be used for TFT gate electrodes, its use has the drawback that chromium has a high electrical resistance [0004]. Ota further teaches that the use of AlOx and TaOx provides better insulation than conventional SiN alone, and prevents pinholes present in the SiN from causing current leaks between the gate and adjacent conductive layers [0005] and [0019].

c. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to have substituted within the Ha device an upper metal layer that is less oxidizable than the lower layer (as taught by Ha) but is still oxidizable to some extent for the purposes of (1) providing a T-shaped gate that reduces current leakage (as taught by Ha) while simultaneously providing a gate electrode that (1) has better insulation properties to prevent pinhole induced leakage between the gate and an adjacent conductive layer as taught by Ota (e.g., between the

gate top and upper wiring layers for top-gate TFTs or between the gate bottom and the laterally-disposed poly-Si for bottom gate TFTs) and/or (2) obviates the need for the additional manufacturing steps required for providing an aligned insulator above the upper-gate layer as required by Ha.

d. Regarding claims 33-38, it would have further been obvious to specifically employ Al for the more oxidizable gate layer and Ta for the less oxidizable layer because Ha teaches that either Al or Ta may be employed for TFT gates, and Ota teaches that Ta has a lower oxidation rate than that of Al.

13. Claims 33-38 are alternatively rejected under 35 U.S.C. 103(a) as being unpatentable over Ha/Ota as applied to the claims above, and further in view of IBM Technical Disclosure Bulletin, "Method of Anodic Oxidation Using Two Metals," March 1995, Vol. 38, No. 03, pp. 441-442. This reference teaches the anodic oxidation of TFT gates composed of two layers of Al and Ta and teaches that Al has a faster oxidation rate than Ta. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to have specifically employed Al and Ta for the materials of oxidizable T-shaped TFT gates taught by Ha/Ota since Ha/Ota teaches that these materials can both be used for TFT gates and that they are both oxidizable, and IBM expressly teaches the relative oxidation rates.

14. Claims 1-3, 6-8, 11-13, 15-18, 20, 29, 30 and 33-38 are alternatively rejected under 35 U.S.C. 103(a) as being unpatentable over Ha/Ota or alternatively Ha/Ota/IBM as applied to the claims above and further in view of Yamazaki '998 (previously made of record in paper #3). Ha/Ota or Ha/Ota/IBM teach all of the elements of the claims, as explained above.

a. Even assuming *arguendo* that insufficient motivation has been proffered for combining these references to produce the resultant invention, Yamazaki teaches TFTs having anodized gate electrodes, albeit not T-shaped, two-layer gates. It would have been obvious to one of ordinary skill in the art at the time of the invention to have combined either of Ha/Ota or alternatively Ha/Ota/IBM in the manner set forth above so as to provide a T-shaped gate having anodic oxidized top and side surfaces for the purpose of providing a gate insulator with high resistivity (e.g., col. 5, lines 1-) and more uniform oxide coverage than that afforded by other conventional insulators (e.g., col. 3, lines 1-18).

INFORMATION ON HOW TO CONTACT THE USPTO

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to the examiner, **B. William Baumeister,** at **(703) 306-9165.** The examiner can normally be reached Monday through Friday, 8:30 a.m. to 5:00 p.m. If the Examiner is not available, the Examiner's supervisor, Mr. Eddie Lee, can be reached at (703) 308-1690. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

B. William Baumeister

Patent Examiner, Art Unit 2815

June 11, 2002